CLAIMS:

1. A multiprocessor system more particularly for terminal devices of mobile radiotelephony in which are arranged on a common chip:

- at least two processors (1, 12),
- at least one rewritable memory (10) to which the two processors (1, 12) can have access,
- at least one cache memory (8, 9) via which the first processor (1) has access to the memory (10), and
- at least one bridge (15) via which the second processors (12) has access to the memory (10).

2. A multiprocessor system as claimed in claim 1, characterized in that the two processors (1, 12) work with mutually different working clocks.

3. A multiprocessor system as claimed in claim 1 ~~or 2,~~ characterized in that the first processor (1) is a digital signal processor (2) and the second processor (12) is a system microcontroller (13).

4. A multiprocessor system as claimed in ~~one of the preceding~~ claim 1, characterized in that the memory (10) is connected to the first processor (1) via two cache memories (8, 9), one of which is used for access to the memory (10) for reading a program and the other of which is used for access to the memory (10) for reading out data.

5. A multiprocessor system as claimed in ~~one of the preceding~~ claim 1, characterized in that in the memory (10) each processor (1, 12) is assigned a separate memory area for a program and for data.

6. A multiprocessor system as claimed in ~~one of the preceding~~ claim 1,

characterized in that the bridge (15) is provided for synchronization between a first data bus (11) via which the memory (10) communicates, and a second data bus (14) via which the second processor (12) communicates and which has a narrower transmission width.

7. A multiprocessor system as claimed in claim 6, characterized in that the data bus (11) assigned to the memory (10) has a transmission width of at least 128 bits and the data bus (14) assigned to the second processor (12) has a transmission width of at least 32 bits.

8. A multiprocessor system as claimed in ~~one of the preceding~~ claims, characterized in that the bridge (15) is provided for managing the access to the memory (10) so that in the case of a conflict of access, preferably the first processor (1) is served.

9. A multiprocessor system as claimed in ~~one of the preceding~~ claims, characterized in that a further data memory (16) integrated on a chip is connected to the second processor (12) via a data bus.

10. A multiprocessor system as claimed in claim 9, characterized in that for enabling an access of the first processor (1) to the further data memory (16) on the chip a DMA controller (17) and a second bridge (18) are provided.

11. A multiprocessor system as claimed in ~~one of the preceding~~ claims, characterized in that ~~the first~~ processor (1) is assigned at least an internal high-speed data memory (5a, 5b) and/or at least an internal high-speed program memory (4).

12. A multiprocessor system as claimed in claim 11, characterized in that the processor sub-system (3) formed by the first processor (1) and the internal memory (memories) has a double Harvard architecture.

13. A multiprocessor system as claimed in ~~one of the preceding~~ claims, characterized in that the memory (10) is an MTP memory or a FLASH memory.

14. A multiprocessor system as claimed in ~~one of the preceding~~ claims,

characterized in that the further data memory (16) of the second processor (12) is a DRAM or SRAM.

15. A multiprocessor system as claimed in ~~one of the preceding~~ claim 1, characterized in that the internal high-speed data memory (5a, 5b) and/or the program memory (4) is a RAM.

16. A use of a multiprocessor system as claimed in ~~one of the~~ claims ~~1 to~~ 15 for the operation of a telecommunication terminal device of mobile radiotelephony.